(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 442 335 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **91101350.6**

(51) Int. Cl.5: **G11C 16/04**, G11C 7/00

(22) Date of filing: **01.02.91**

(30) Priority: **01.02.90 JP 20442/90**

(43) Date of publication of application:
21.08.91 Bulletin 91/34

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **Kabushiki Kaisha Toshiba**
72, Horikawa-cho Saiwai-ku
Kawasaki-shi(JP)

(72) Inventor: **Uemura, Teruo, c/o Intellectual Property Division**
Kabushiki Kaisha Toshiba, 1-1 Shibaura 1-chome
Minato-ku, Tokyo 105(JP)
Inventor: **Kawase, Yukio, c/o Intellectual Property Division**
Kabushiki Kaisha Toshiba, 1-1 Shibaura 1-chome
Minato-ku, Tokyo 105(JP)

(74) Representative: **Lehn, Werner, Dipl.-Ing. et al**
Hoffmann, Eitle & Partner Patentanwälte
Arabellastrasse 4
W-8000 München 81(DE)

(54) Semiconductor memory device including nonvolatile memory cells, enhancement type load transistors, and peripheral circuits having enhancement type transistors.

(57) A semiconductor memory device comprises a non-volatile memory cell array (70) having a plurality of memory cells (71), enhancement type load transistors (73, 73') having a threshold voltage, and at least one peripheral circuit, such as level shifters (74), column decoders (76), etc., including enhancement type transistors having a threshold voltage. For increasing the writing speed of the memory cells (71), the threshold voltage of the enhancement type load transistors (73, 73') is set so that it is different from that of the enhancement type transistors of the peripheral circuit. For example, the threshold voltage of the enhancement type load transistors (73, 73') is lower than that of the enhancement type transistors of the peripheral circuit.

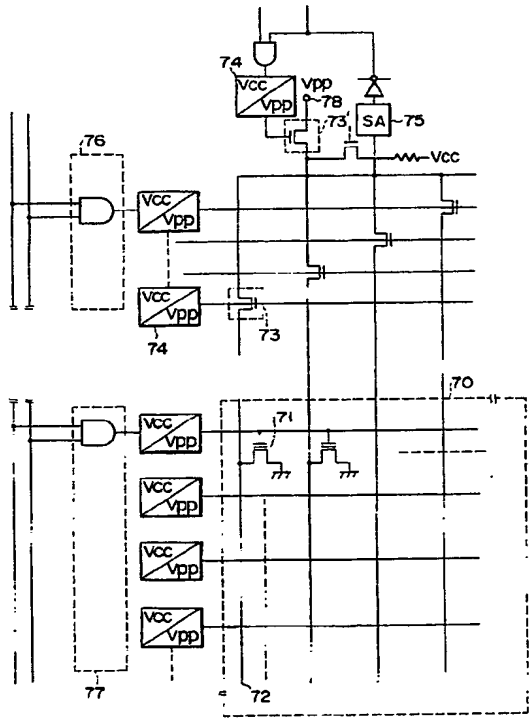

FIG. 3

EP 0 442 335 A1

SEMICONDUCTOR MEMORY DEVICE INCLUDING NONVOLATILE MEMORY CELLS, ENHANCEMENT TYPE LOAD TRANSISTORS, AND PERIPHERAL CIRCUITS HAVING ENHANCEMENT TYPE TRANSISTORS

This invention relates to a semiconductor memory device, and more particularly to a semiconductor memory device including nonvolatile memory cell transistors.

EPROMs (Erasable Programmable Read Only Memory), i.e., charge-injection type nonvolatile semiconductor devices, have been manufactured by such a method as is shown in Figs. 5A - 5D. In these figures, broken line 101 indicates the border between a memory cell and a load transistor, and broken line 102 the border between the load transistor and a peripheral circuit.

In the method, at first, a field oxide film 42 and a gate oxide film 43 are provided on a semiconductor substrate 41 as shown in Fig. 5A. The semiconductor substrate surface is coated with a resist layer 44 as shown in Fig. 5B. Using photolithography techniques, the resist film 44 is selectively removed to provide a window 46 for forming a channel region 45 of the memory cell transistor therein. Subsequently, impurity ions are implanted into the substrate through the window 46, followed by removing the resist film 44. As shown in Fig. 5C, the substrate surface is coated with a resist film 47, and using photolithography techniques, the resist film 47 is selectively removed to provide windows 50 and 51 for forming channel regions 48 and 49 of the load transistor and peripheral transistor, respectively. Thereafter, impurity ions are implanted into the substrate through these windows 50 and 51, and then the resist film 47 is removed. Finally, as shown in Fig. 5D, a floating gate 52, an oxide film 53 (provided between control and floating gates), a control gate 54, gate electrodes 55, diffused regions 56, an insulating film 57, an Al wiring layer 58, and a passivation film 59 are successively provided.

The channel regions of the load transistors are formed by the same impurity ion implantation process (the same dose) as that of making the channel regions of enhancement type transistors used in peripheral circuits. Accordingly, each load transistor has a threshold voltage equal to that of each enhancement type transistor.

The semiconductor memory device described above, however, has the following disadvantage.

In general, the peripheral circuit includes at least one enhancement type transistor whose source potential is different from the substrate potential. The substrate is then biased relative to the source of the enhancement type transistor. Therefore, the threshold voltage may be increased under an operating condition in the enhancement type transistor of the peripheral circuit. The threshold voltage is usually measured in a state in which the source and the substrate of the transistor are kept at the same potential. The threshold voltage may be also increased in each enhancement type load transistor connected to each memory cell transistor, because the source of the load transistor is not kept at the same potential as that of the substrate. In the enhancement type load transistor connected to the memory cell transistor, a voltage drop corresponding to the threshold voltage (Vth) may occur, which will make the voltage applied to the memory cell transistor lower than the voltage applied to a power supply voltage terminal. When the voltage applied to the memory cell transistor is lowered, the electric field between the drain and source regions may be decreased to reduce the quantity of generated carrier. Consequently, the writing speed to the memory cell may be lowered.

On the one hand, since current leakage occurs between the source and drain regions of the transistors in the peripheral circuits, it cannot be possible to set the threshold voltage of each enhancement type transistor at a low value. On the other hand, each enhancement type load transistor has a comparatively long gate length (L poly), the problem of the current leadkage may not occur. Therefore, it may be possible to set the threshold voltage at a low value.

As described above, in the conventional semiconductor memory device including charge-injection type nonvolatile memory cell transistors, the voltage applied from the power supply may be greatly lowered in the enhancement type load transistors, thereby decreasing the writing speed into the memory cells.

It is an object of the invention to provide a semiconductor memory device having a high writing speed.

It is another object of the invention to provide a semiconductor memory device in which a voltage supplied from a power supply is not greatly lowered by load transistors incorporated therein.

According to one aspect of the present invention, there is provided a semiconductor memory device which comprises a nonvolatile memory cell array having a plurality of memory cells, enhancement type load transistors having a threshold voltage, and at least one peripheral circuit, such as level shifters, column decoder, etc., including enhancement type transistors having a threshold voltage. For increasing the writing speed of the memory cells, the threshold voltage of each of the enhancement type load transistors is set so that it is different from that of the enhancement type

transistors of the peripheral circuit. For example, the threshold voltage of enhancement type load transistors is lower than that of the enhancement type transistors of the peripheral circuit.

The novel and distinctive features of the invention are set fourth in the claims appended to the present application. However, the invention together with further objects and advantages thereof may best be understood by reference to the following description and accompanying drawings in which:

Figs. 1A through 1E are partial sectional views for explaining a semiconductor memory device and control of a threshold voltage of circuit elements according to one embodiment of the present invention;

Figs. 2A and 2B are graphs showing the characteristics of the semiconductor memory device according to the embodiment of the present invention;

Fig. 3 is a circuit diagram showing a structure of the semiconductor memory device according to the embodiment of the present invention;

Figs. 4A and 4B are circuit diagrams showing peripheral circuits shown in Fig. 3; and

Figs. 5A through 5D are partial sectional views for explaining control of a threshold voltage of circuit elements in a conventional semiconductor memory device.

A semiconductor memory device according to an embodiment of the present invention will be described in detail with reference to the drawings.

In Figs. 1A through 1E, broken line 1 indicates the border between a memory cell and a load transistor, and broken line 2 the border between the load transistor and a peripheral circuit, respectively.

As shown in Fig. 1A, a field oxide film 12 and a gate oxide film 13 are formed on a semiconductor substrate 11 by means of LOCOS (Local Oxidation of Silicon) techniques.

Then, as shown in Fig. 1B, after the substrate surface is coated with a resist film 14, using photolithography techniques the resist film 14 is selectively removed to provide a window 16 for forming a channel region 15 of the memory cell transistor therein. Subsequently, impurity ions are implanted into the substrate through the window 16, followed by removing the resist film 14.

As shown in Fig. 1C, the substrate surface is coated with a resist film 17, and using photolithography techniques the resist film 17 is selectively removed to provide a window 19 for forming a channel region 18 of the load transistor therein. Thereafter, an ion implatation is carried out through the window 19 so that the threshold voltage of the load transistor may become 0.6 V, and the resist film 17 is removed from the substrate surface.

Subsequently, as shown in Fig. 1D, the substrate surface is coated with a resist film 20, and using photolithography techniques the resist film 20 is selectively etched to provide a window 22 for forming a channel region 21 of an enhancement type transistor included in peripheral circuits. Impurity ions are implanted into the substrate so that the threshold voltage of the enhancement type transistor may become 0.8 V. The resist film 20 is then removed from the substrate surface.

Finally, as shown in Fig. 1E, a floating gate 23, a control gate 25, an oxide film 24 provided between the gates 23 and 25, gate electrodes 26, diffused regions 27 (source and drains regions), an insulating films 28, an A1 wiring layer 29, and a passivation film 30 are successively provided.

In the present invention as described above, the channel regions of both the enhancement type load transistor and the enhancement type transistor in the peripheral circuit are subjected to the different ion implantation processes to control the threshold voltage thereof, while they are subjected to the same ion implantation process in the convention device.

The power consumption of the memory cell transistors can be reduced when the threshold voltage of each enhancement type load transistor connected to each memory cell transistor is made higher than that of each enhancement type transistor included in the peripheral circuits.

Further, even if a semiconductor memory device includes 5 V system transistors and high voltage system transistors to render a different thickness in their gate oxide films, a semiconductor substrate may be subjected to different ion implantation processes to provide channel regions for load transistors, 5 V system transistors and high voltage system transistor, respectively.

Fig. 2A shows a static characteristic 31 of the EPROM cell and load characteristics 32 of the load transistor. In this figure, Vpp is the voltage applied between source and drain regions of the memory cell, and Ipp is the current flowing therebetween. A1 and A2 indicate an operating point of a writing circuit and a voltage applied to the drain region of the cell when the load transistor has the threshold voltage of 0.8 V, respectively. B1 and B2 indicate the operating point of the writing circuit and the voltage applied to the drain region of the cell when the load transistor has the threshold voltage of 0.6 V, respectively. As can be understood from the graph, when the threshold voltage of the load transistor is low, the current Ipp flowing through the cell at the operating point of the writing circuit may be increased. Therefore, the writing characteristic of the memory cells may be improved. Fig. 2B shows the writing characteristics as an improvement of a writing speed. In the figure, tpw is the writing time into the memory cell, and Vth is the

threshold voltage of the memory cell. Curves T_A and T_B indicate the writing characteristic when the threshold voltage of the load transistor is 0.8 v and 0.6 V, respectively. The time required for that the threshold voltage of the memory cell transistor reaches a sense level (Ls), that is, the writing time is given by 300 μs in T_A and by 60 μs in T_B, respectively. Accordingly, if the threshold voltage is decreased by 0.2 V only, the writing speed may be increased by 5 times.

Fig. 3 shows a circuit configuration of the EPROM, which includes an array 70 of charge-injection type memory cell transistors 71, enhancement type load transistors 73 for selecting respective columns 72, level shifters 74, a sense amplifier 75, column decoders 76, row decoders 77, and the like. In Fig. 3, the enhancement type transistors 73 and 73' are enhancement type load transistors for the charge-injection type non-volatile memory cell transistors 71. The level shifters 74 and column decoders 76 are connected to the enhancement type load transistors and provide one of the peripheral circuits including enhancement type transistors.

A voltage Vpp (e.g. 12 V) is applied to the enhancement type load transistors 73 and 73' through a power supply voltage terminal 78 to perform writing to a desired memory cell transistor 71. For carrying out a reading operation of the memory cell transistor 71, a voltage Vcc (e.g. 5 V) is applied through the corresponding enhancement type load transistor 73 thereto.

Figs. 4A and 4B show one example of the known level shifter 74, and decoders 76 and 77, shown in Fig. 3, which provide the peripheral circuits. These circuits include enhancement type field effect transistors.

Specifically, in the level shifter 74 shown in Fig. 4A, a first series circuit, comprised of an N-channel transistor T1 and a P-channel transistor T2, and a second series circuit, comprised of an N-channel transistor T3 and a P-channel transistor T4, are connected in parallel between a power supply voltage (Vpp) terminal and a ground terminal. The connection point between the transistors T1 and T2 is connected to the gate of the transistor T3, while the connection point between the transistors T3 and T4 is connected to the gate of the transistor T1. Further, a inverter comprised of an N-channel transistor T5 and a P-channel transistor T6 is connected between a power supply voltage (Vcc) terminal and a ground terminal. The gates of the transistors T5 and T6 are connected to the gate of the transistor T2 in common, while the connection point between the transistors T5 and T6 is connected to the gate of the transistor T4. An input terminal 411 is connected to the gate of the transistor T2, and an output terminal 412 is connected to the connect between the transistors T3 and T4. Upon supply of an input signal, the voltage Vpp is fed from the output terminal 412.

The decoders 76 and 77 shown in Fig. 4B have the same circuit configuration. In the decoder, P-channel transistors T3 and T4 are connected in series with a parallel circuit comprised of N-channel transistors T1 and T2. The gate of the transistor T3 is connected to the gate of the transistor T1 connected to a first input terminal 421, and the gate of the transistor T4 is connected to the gate of the transistor T2 connected to a second input terminal 422, thereby providing a NAND circuit. The NAND circuit is connected in series with an inverter provided by an N-channel transistor T5 and a P-channel transistor T6. The connection point between the transistors T5 and T6 is connected to an output terminal 423. A power supply Vcc/vpp is connected to one end of the transistors T1, T2 and T5 to perform a described operation.

The present invention can be also applied in the case where the threshold voltage of the enhancement type load transistor is different from a threshold voltage of each enhancement type transistor included in the sense amplifiers or in I/O buffers.

Further, the present invention is not limited to the EPROM mentioned above, but it will be applicable to EEPROMs (Electrically Erasable and Programmable Read Only Memories).

According to the present invention as described above, in the semiconductor memory device including charge-injection type nonvolatile memory cell transistors, the voltage supplied from the power supply will not be greatly lowered by the enhancement type load transistors, resulting in the high writing speed.

It is further understood by those skilled in the art that the foregoing description is a preferred embodiment of the disclosed device and that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

Claims

1. A semiconductor memory device comprising a semiconductor substrate (11) including a non-volatile memory cell array (70), enhancement type load transistors (73, 73') having a threshold voltage, and at least one peripheral circuit (74, 76, 77) including enhancement type transistors having a threshold voltage,

characterized in that said threshold voltage of said enhancement type load transistors (73, 73') is different from that of said enhancement type transistors of said peripheral circuit (74, 76, 77).

2. The semiconductor memory device according to claim 1,
characterized in that said threshold voltage of said enhancement type load transistors (73, 73') is lower than that of said enhancement type transistors of said peripheral circuit (74, 76, 77).

3. The semiconductor memory device according to claim 2,
characterized in that said threshold voltage of said enhancement type load transistors (73, 73') is approximately 0.6 V, while said threshold voltage of said enhancement type transistors of said peripheral circuit (74, 76, 77) is approximately 0.8 V.

4. The semiconductor memory device according to claim 1,
characterized in that said semiconductor substrate has power supply voltage terminals.

5. The semiconductor memory device according to claim 1,
characterized in that said nonvolatile memory cell array (70) includes a plurality of memory cell transistors (71) each having a source and a drain.

6. The semiconductor memory device according to claim 1,
characterized in that each of said enhancement type load transistors (73, 73') has a source, a drain and a gate.

7. The semiconductor memory device according to claim 1,
characterized in that each of said enhancement type transistors of said peripheral circuit (74, 76, 77) has a source and a drain.

8. The semiconductor memory device according to claim 1,
characterized in that said peripheral circuit includes at least level shifters (74) and column decoders (76).

9. The semiconductor memory device according to claim 6,
characterized in that one of said source and drain in each of said enhancement type load transistors (73) is connected to one of said power supply voltage terminals (78).

10. The semiconductor memory device according to claim 5,
characterized in that one of said source and drain in each of said memory cell transistors (71) is connected to the other of said source and drain in each of said enhancement type load transistors (73).

11. The semiconductor memory device according to claim 1,
characterized in that said peripheral circuit (74) is connected to said gate of each of said enhancement type load transistors (73).

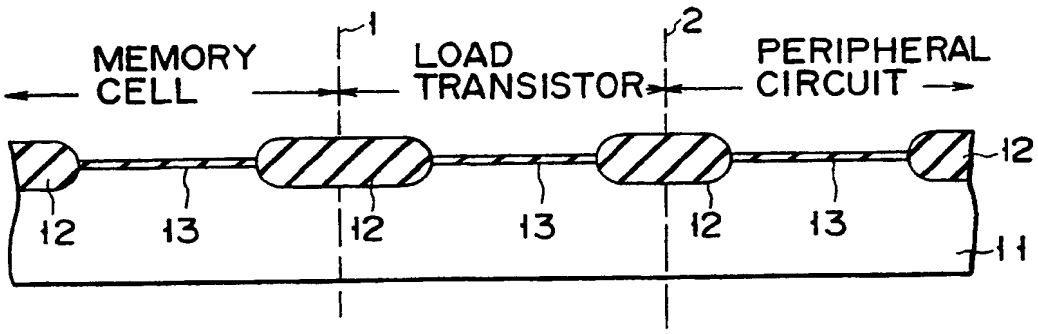

FIG. 1A

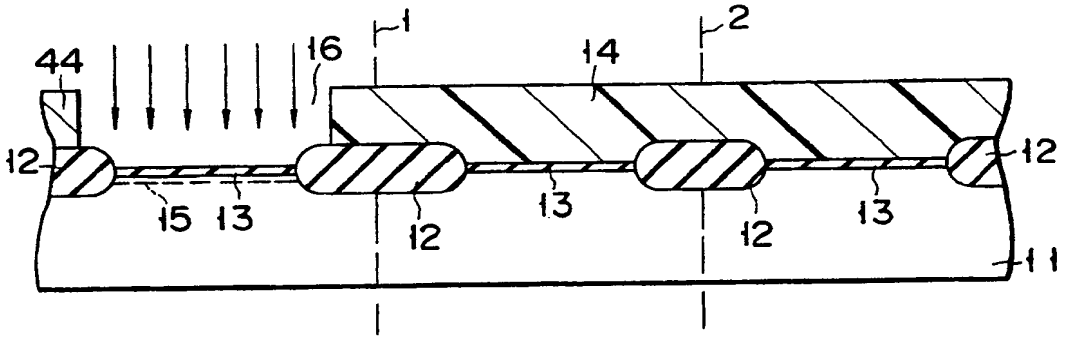

FIG. 1B

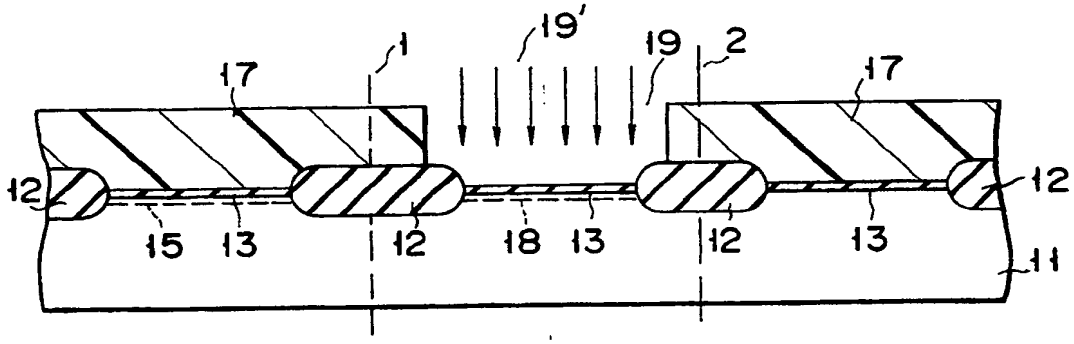

FIG. 1C

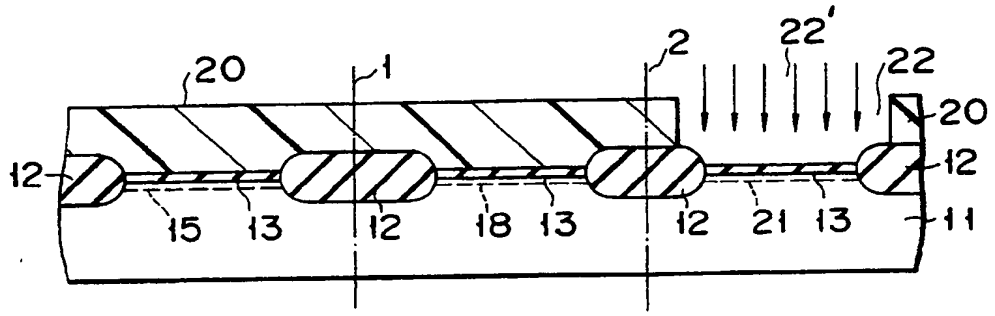

FIG. 1D

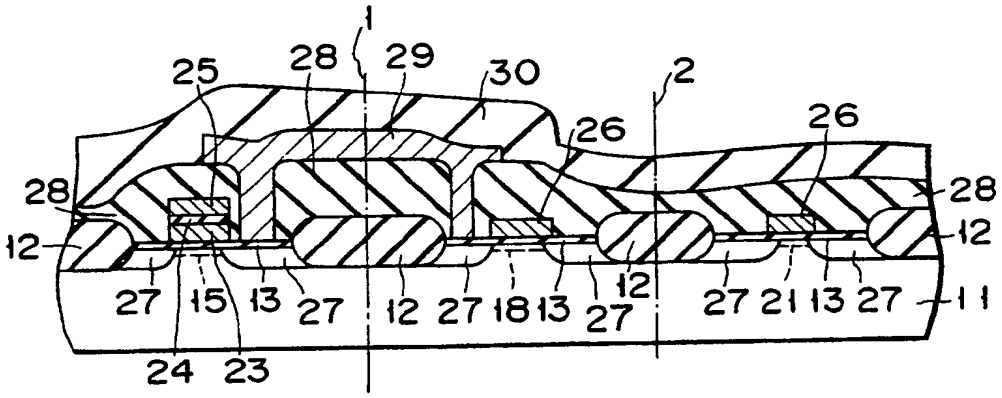

FIG. 1E

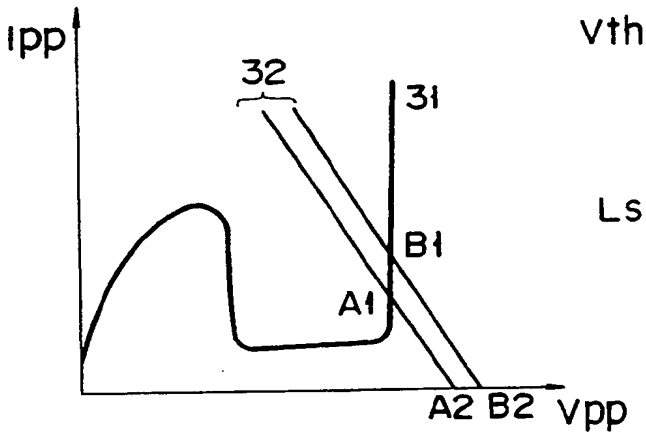

FIG. 2A

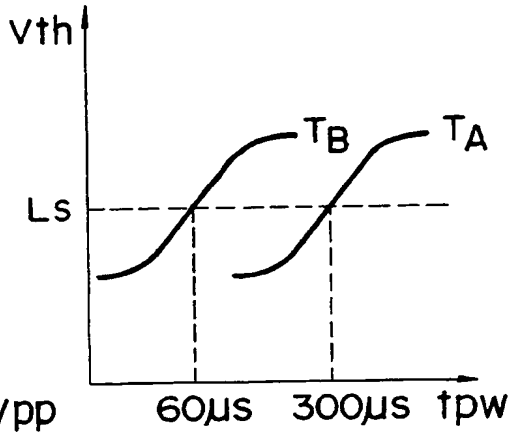

FIG. 2B

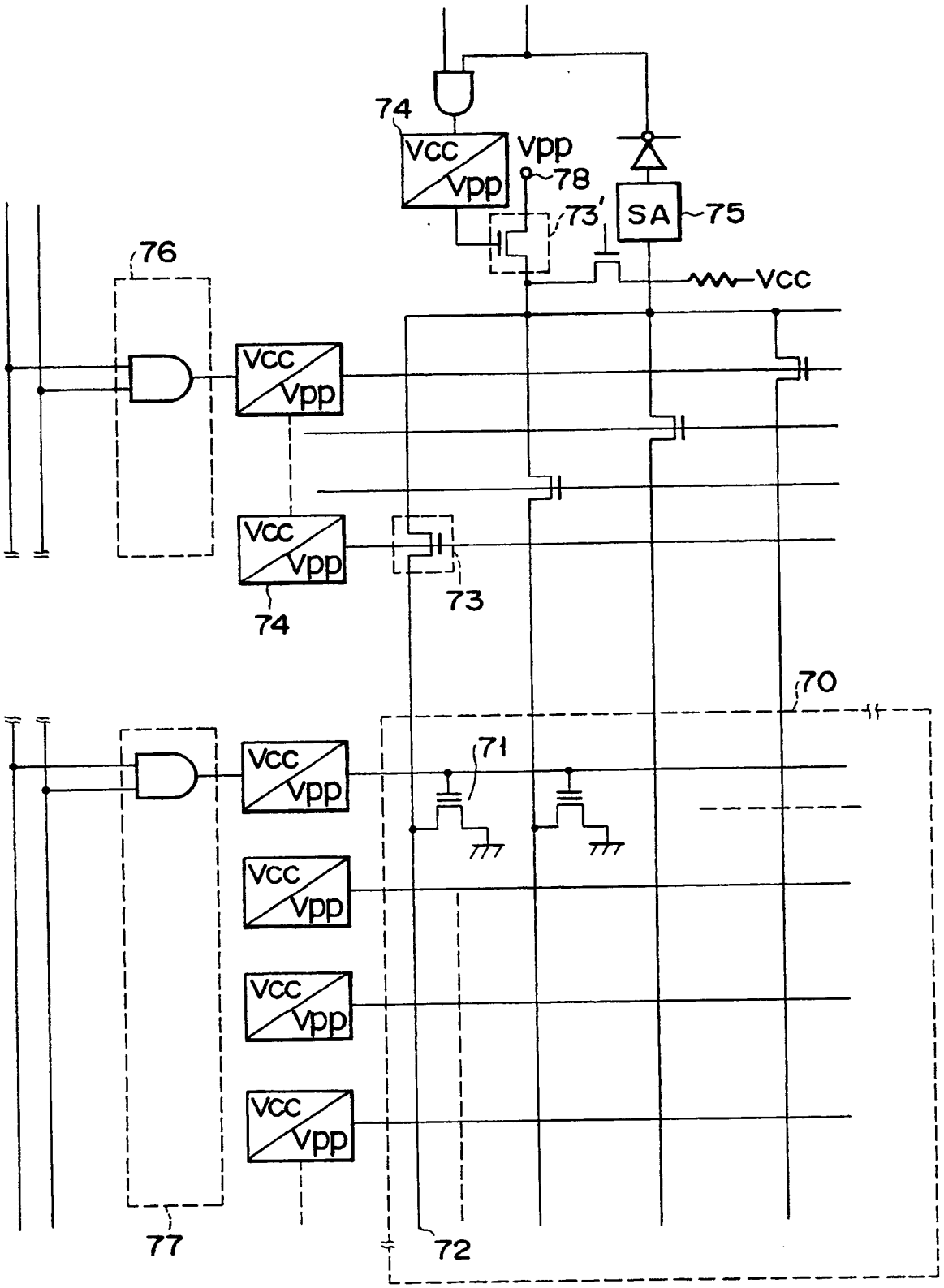

FIG. 3

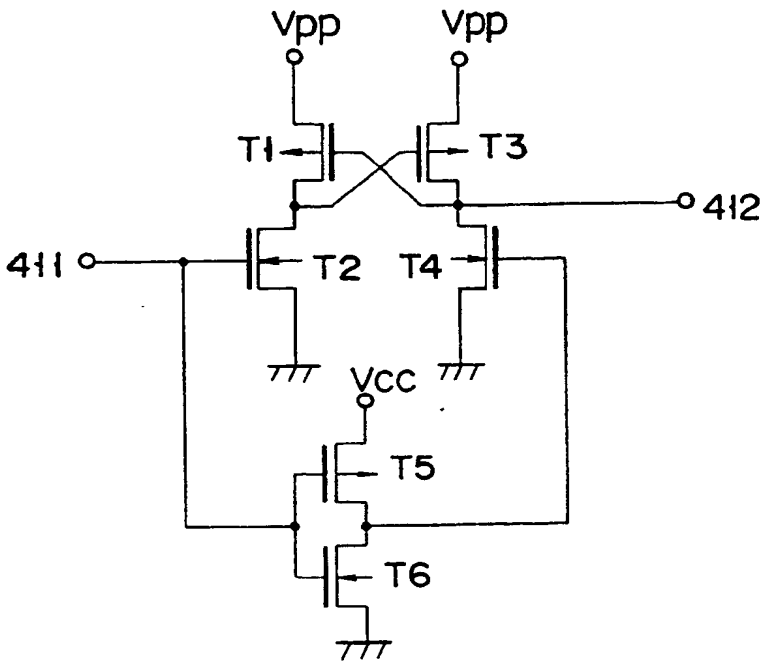

FIG. 4A

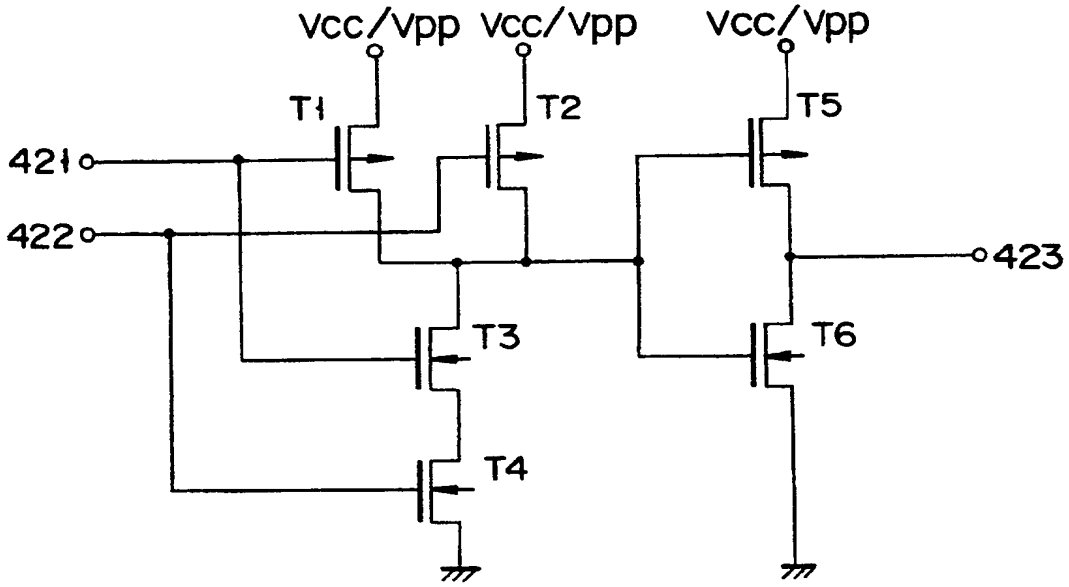

FIG. 4B

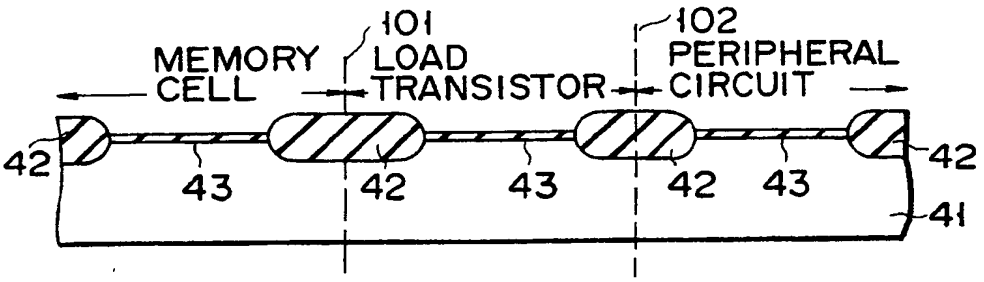

FIG. 5A

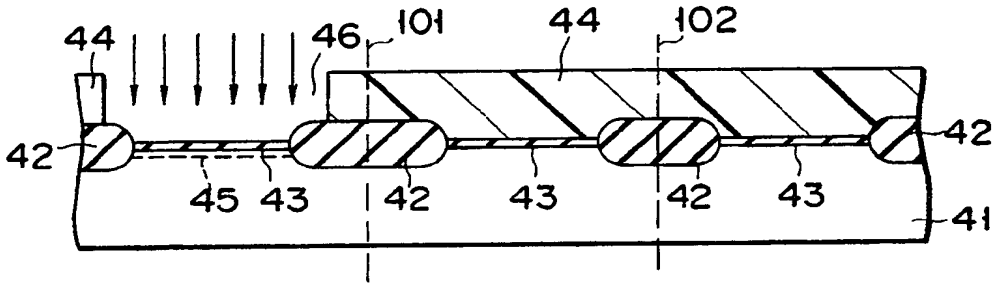

FIG. 5B

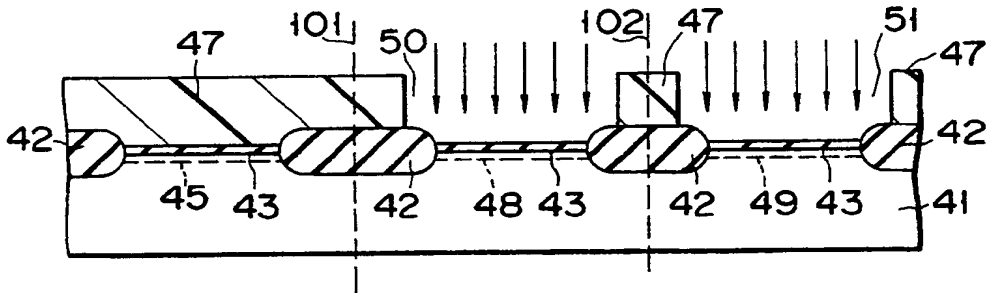

FIG. 5C

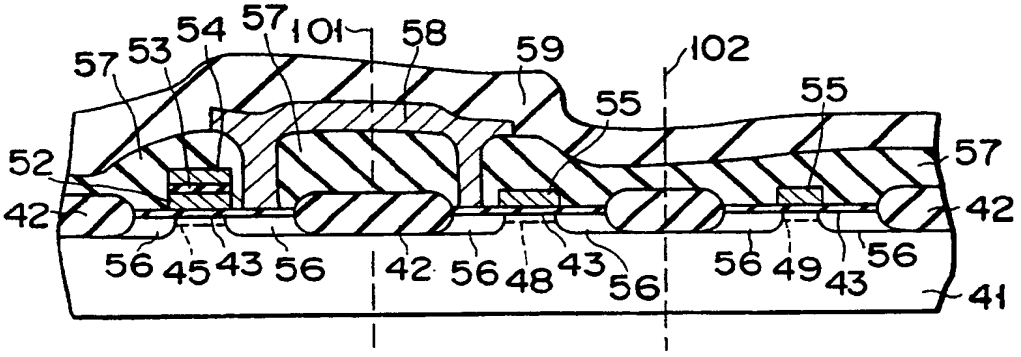

FIG. 5D

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 91101350.6

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US - A - 4 575 823 (FITZPATRICK) * Abstract; column 1, line 15 - column 3, line 21; claim 1; fig. 11B *	1	G 11 C 16/04 G 11 C 7/00
A	US - 4 571 705 (WADA) * Abstract; columns 1,2; claim 1; fig. 8 *	1	
A	US - A - 4 751 678 (RAGHUNATHAN) * Abstract; column 1, lines 5-10; claim 1; fig. 1 *	1	
A	US - A - 4 813 018 (KOBAYASHI)	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	04-06-1991	GRÖSSING

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)